IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Garg et al.

Appl. No.: To be assigned

Filed: September 22, 1997

For:

RISC Microprocessor

Architecture Implementing Multiple Typed Register Sets

Art Unit: To be assigned

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Examiner: To be assigned

Atty. Docket: SP018.C3

Preliminary Amendment

Assistant Commissioner for Patents Washington, D.C. 20231

Sir:

Prior to examining the above captioned application, please enter the following Amendment.

It is believed that extensions of time or fees for net addition of claims are not required beyond those which may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to our Deposit Account No. 19-0036.

Kindly enter the following amendments:

In the Specification:

Page 1, please delete lines 18-21 and insert the following:

--1. High-Performance, Superscalar-Based Computer System with Out-of-Order Instruction Execution, Appl. No. 07/817,810, filed Jan 8, 1992, now U.S. Patent No. 5,539,911, by Le Trong Nguyen *et al.*;

K1 H2